AMENDMENTS TO THE CLAIMS

1. – 60. (Canceled).

61. (Currently amended) A method of forming a memory element, said method comprising:

forming a first electrode;

forming ~~at least one~~ a first resistance variable material layer in contact with the first electrode;

forming ~~at least one~~ a first metal-containing layer adjacent said resistance variable material;

forming a metal layer in contact with the first metal-containing layer;

forming a second electrode in contact with the metal layer; and

forming at least one conducting channel within said resistance variable material layer by applying a conditioning voltage to the memory element~~, wherein said conditioning voltage has a pulse duration of from about 10 to about 500 ns and is approximately 700 mV or greater~~.

62. (Original) The method of claim 61, wherein said resistance variable material layer is a chalcogenide glass layer.

63. (Original) The method of claim 62, wherein said chalcogenide glass layer has a stoichiometry of Ge_xSe_{100-x}.

64. (Original) The method of claim 63, wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{18}Se_{82}$ to $Ge_{25}Se_{75}$.

65. (Original) The method of claim 64, wherein said chalcogenide glass layer is doped with metal ions.

66. (Original) The method of claim 65, wherein said metal ions are silver ions.

67. (Original) The method of claim 66, wherein said doped chalcogenide glass layer is from about 150 Å to about 600 Å thick.

68. (Original) The method of claim 67, wherein said doped chalcogenide glass layer has polarizable metal-chalcogen regions.

69. (Original) The method of claim 68, wherein said polarizable metal-chalcogen regions are Ag_2Se regions within a germanium-selenide glass backbone.

70. (Original) The method of claim 69, wherein said Ag_2Se regions become aligned upon application of said conditioning voltage to said memory element.

71. (Original) The method of claim 70, wherein said conditioning voltage is greater than subsequent write, read, and erase voltages.

72. (Original) The method of claim 70, wherein the Ag_2Se regions form at least one conducting channel by becoming polarized and aligning within the doped chalcogenide glass layer.

73. (Original) The method of claim 61, wherein prior to applying said conditioning voltage, said memory element has a first resistance state and after

applying said conditioning voltage to said memory element, said memory element has a second resistance state lower than said first resistance state.

74. (Original) The method of claim 73, wherein subsequent write, read, and erase voltages have an absolute magnitude lower than that of said conditioning voltage.

75. (Original) The method of claim 74, wherein applying a write voltage produces a third resistance state lower than the second resistance state.

76. (Original) The method of claim 75, wherein applying a second write voltage produces a fourth resistance state lower than said third resistance state.

77. (Original) The method of claim 61, wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{20}Se_{80}$ to $Ge_{43}Se_{57}$.

78. (Original) The method of claim 77, wherein said chalcogenide glass layer has a stoichiometry of $Ge_{40}Se_{60}$.

79. (Original) The method of claim 77, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick.

80. (Currently amended) The method of claim 61, wherein said ~~at least one~~ a first metal-containing layer is from about 300 Å to about 1200 Å thick.

81. (Currently amended) The method of claim 80, wherein said ~~at least one~~ a first metal-containing layer is an Ag_2Se layer.

82. (Original) The method of claim 81, wherein the conditioning voltage is applied to the memory element driving Ag_2Se into the chalcogenide glass layer.

83. (Canceled).

84. (Previously Presented) The method of claim 82, wherein the chalcogenide glass layer has a germanium-selenide glass backbone.

85. (Original) The method of claim 84, wherein the Ag_2Se bonds to the germanium-selenide glass backbone forming at least one conducting channel within said chalcogenide glass layer.

86. (Original) The method of claim 80, further comprising forming a second metal-containing layer over the first metal-containing layer.

87. (Original) The method of claim 86, wherein said second metal-containing layer comprises silver ions.

88. (Original) The method of claim 87, wherein said silver ions are driven into and out of the at least one conducting channel by applying different voltages.

89. -98. (Canceled).

99. (Currently amended) A method of forming a memory element, said method comprising:

forming ~~at least one~~ a first chalcogenide glass layer;

forming ~~at least one~~ a first metal-containing layer over said chalcogenide glass layer;

forming a second chalcogenide glass layer over the first metal-containing layer;

forming a second metal-containing layer over the first ~~metal-containing~~chalcogenide glass layer;

electrically coupling first and second electrodes to said first and second chalcogenide glass ~~layer~~ layers, wherein the second electrode is formed in contact with said second metal-containing layer; and

applying a conditioning pulse to the memory element to bond regions of metal and glass within at least one of said first and second chalcogenide glass ~~layer~~ layers, said bonded regions forming at least one conducting channel within said at least one of said first and second chalcogenide glass ~~layer~~ layers.

100. (Original) The method of claim 99, wherein said chalcogenide glass layer has a stoichiometry that is from about $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$.

101. (Original) The method of claim 100, wherein said chalcogenide glass layer has a stoichiometry that is $Ge_{40}Se_{60}$.

102. (Original) The method of claim 100, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick.

103. (Original) The method of claim 99, wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick.

104. (Original) The method of claim 103, wherein said at least one metal-containing layer is an Ag_2Se layer.

105. (Original) The method of claim 102, wherein said chalcogenide glass has a germanium-selenide glass backbone.

106. (Original) The method of claim 105, wherein the bonded regions of metal is Ag_2Se bonded to germanium-selenide.

107. (Original) The method of claim 99, wherein the memory element has a first resistance state.

108. (Original) The method of claim 107, wherein applying a write voltage moves said memory element from said first resistance state to a second resistance state, said second resistance state being lower than said first resistance state.

109. (Original) The memory element of claim 108, wherein applying a second write voltage to said memory element moves said memory element from said second resistance state to a third resistance state, said third resistance state being lower than said second resistance state.

110. (Canceled).

111. (Previously Presented) The method of claim 99, wherein said second metal-containing layer comprises silver ions.

112. (Original) The method of claim 111, wherein said silver ions are driven into and out of the at least one conducting channel by applying a write, erase or read voltage.

113. (Original) The method of claim 99, further comprising forming a second chalcogenide glass layer over said at least one metal-containing layer.

114. (Original) The method of claim 113, wherein said second chalcogenide glass layer is from about 100 Å to about 300 Å thick.

115. (Canceled).

116. (Currently amended) ~~The method of claim 115~~ A method of forming a memory element, said method comprising:

forming a first chalcogenide glass layer;

forming a first metal-containing layer over said chalcogenide glass layer;

forming a second chalcogenide glass layer over the first metal-containing layer;

forming a second metal-containing layer over the second chalcogenide glass layer, wherein said second metal-containing layer is from about 100 Å to about 500 Å thick;

electrically coupling first and second electrodes to said first chalcogenide glass layer; and

applying a conditioning pulse to the memory element to bond regions of metal and glass within said chalcogenide glass layer, said bonded regions forming at least one conducting channel within said chalcogenide glass layer.

117. (Canceled) The method of claim 116, further comprising forming a third metal-containing layer over said second metal-containing layer.

118. (Original) The method of claim 117, wherein said third metal-containing layer comprises silver ions.

119. (Original) The method of claim 118, wherein said silver ions are driven into and out of the at least one conducting channel by applying a write, erase, or read voltage.

120. – 148. (Canceled).

149. (New) The method of claim 61, wherein said conditioning voltage has a pulse duration of from about 10 to about 500 ns and is approximately 700 mV or greater.